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Vertical Electrical Behaviour of Amorphous and Crystalline Si/Ge and SiGe/Si Structures

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Our recent experimental results concerning the vertical current-voltage and capacitance-voltage behaviour of structures with different amorphous Si/Ge multilayers and amorphous, polycrystalline and epitaxial SiGe layers grown on Si substrates, are summarized.

I. INTRODUCTION

During the last two decades SiGe became an important material for microelectronics and optoelectronics. In this paper our recent experimental results obtained in different Si/Ge structures are summarized.

II. EXPERIMENTAL

All the studied Si/Ge and SiGe/Si structures were prepared on Si substrates. Four different types of structures were studied: A) amorphous Si/Ge multilayers and mixed amorphous SiGe layers sputtered from Si and Ge targets, B) amorphous SiGe layers sputtered from a SiGe target, C) epitaxial SiGe layers grown by molecular beam epitaxy (MBE), and D) multilayered low dimensional SiGe/Si structures grown by MBE. (Details see below.)

Al was evaporated on both the front and backside of the most wafers for the formation of Schottky and ohmic contacts, respectively [1,2]. Square diodes with an area of 0.64 mm^2 were formed on

the front side of the wafers by standard photolithography. On the front side of a few SiGe/Si structures epitaxial $\text{ErSi}_{1.7}$ layers were grown for the electrical contact.

The electrical characteristics were studied by d.c. current-voltage (I-V) measurements, and capacitance voltage (C-V) and conductance-voltage (G-V) measurements at a frequency of 1 MHz in the temperature range of 80-320 K in dark.

A. Amorphous Si/Ge multilayers and mixed amorphous SiGe layers

The amorphous Si/Ge multilayers were grown on p-type Si wafers with the native oxide remaining, in a dual target unbalanced magnetron dc sputtering system. As sputtering gas pure Ar was used. Starting with Si, the shutters were then opened and closed to form the desired multilayer. Between each layer both shutters were closed for 0.25 s [3,4]. The multilayers were grown to a total thicknesses of $0.3 \mu\text{m}$ with a period of 3 nm (100 periods) and 6 nm (50 periods), and were always terminated with an a-Si

layer. Three different bias values were used during sputtering: 0, 140 and 450 V. According to our earlier measurements performed by cross-sectional transmission electron microscopy, sputtering at zero bias yielded amorphous multilayers with pronounced columnar microstructure. Sputtering at a bias of 140 V resulted in more dense and well-defined amorphous multilayers, while homogeneous intermixed amorphous SiGe layers were obtained at a bias of 450 V [3,4].

Two structures grown at a bias of 140 V and 450 V were annealed at 650 °C and 600 °C, respectively, for 10 min in forming gas. Due to the higher annealing step, a polycrystalline SiGe layer was obtained with an average grain size of approximately 50 nm. The other structure remained amorphous [3,4].

B. Amorphous SiGe Layers

The amorphous SiGe layers deposited from a SiGe polycrystalline target were sputtered on both n- and p-type Si substrates. The Ge content of the target was about 6%, but due to Rutherford backscattering measurements, the Ge content in the sputtered films was 4% only [5].

Two different methods of Si surface preparation was used before sputtering. The "Acetone" treatment consisted of consecutive boiling the wafer in new clean acetone three times for 5-5 min. The "HF" treatment consisted of two steps: 1) Cleaning in 1:1 solution of H₂SO₄ and H₂O₂ for 30 min. 2) Etch in 1:20 solution of HF and H₂O for 1 min.

For study the effect of the layer thickness, SiGe layers with thickness in the range of 240-900 nm were deposited onto p-type substrates using the "Acetone" treatment. The effect of hydrogenation was also studied introducing 0.4 % H⁺ into the plasma during deposition ("Acetone" treatment, 900 nm) [6]. The effect of "Acetone" vs. "HF" treatments was studied on both n- and p-type substrates with a layer thickness of 900 nm.

C. Epitaxial SiGe Layers

The epitaxial SiGe layers were grown by MBE with solid phase Si and gas phase GeH₄ sources

on both n- and p-type Si substrates [2,7,8]. First a 0.8 μm thick Si buffer layer was grown. The Ge content in the SiGe layers was in the range of 0.11-0.20. The thickness of the epitaxial layers in the studied structures was in the range of 200-240 nm with a free electron concentration of $3 \times 10^{15} \text{ cm}^{-3}$.

The effect of two different surface treatments performed before Al evaporation, was studied: the "HF" and the "H₂SO₄ + H₂O₂" treatment [2]. These treatments were applied to Si in our earlier work [9]. The "HF" treatment described above is standard in our Si technology. The "H₂SO₄ + H₂O₂" treatment consisted of steps 1) and 2) of the standard "HF" treatment, and as a third step, step 1) was repeated for 15 min.

D. Multilayered SiGe/Si Structures

The multilayered SiGe/Si structures were also grown by MBE [7,8,10,11]. The effect of "HF" vs. "H₂SO₄ + H₂O₂" treatment was studied on the vertical electrical behaviour of high electron mobility transistor (HEMT) structures [7,8] using Al electrical contacts.

In another experiment ErSi_{1.7} epitaxial layers were grown for preparation of ohmic contact to thin SiGe layers with 20 % Ge content [10-13]. 20 nm Er was evaporated onto the wafers and annealed at 500 °C for 5 min in vacuum. Two different wafers were studied. Both of them contained a 20 nm thick SiGe layer grown epitaxially on (100) n-Si. One of the structures contained a 10 nm thick epitaxial Si capping layer, the other was without capping layer [13].

III. RESULTS AND DISCUSSION

A. Amorphous Si/Ge Multilayers and SiGe Layers

Although a significant influence of the preparation, composition and microstructure was obtained on the electrical behaviour of the studied amorphous and multicrystalline structures [1,14] sputtered from Si and Ge targets, most of them exhibited similar specific features. As a common picture, the I-V characteristics of the amorphous and

polycrystalline structures consisted of four different parts [1,14,16]. The first part at low biases showed ohmic behaviour and was connected with a parallel conductance due to hopping mechanism. However, the I-V characteristics of annealed structures did not contain this part. The central, most abrupt part is attributed to a Schottky barrier formed by Al on the amorphous layers. The third part exhibited a near-linear $\log I$ -V relationship with a lower slope at relatively high biases. In this part the current exhibited a parabolic dependence on the bias indicating that the current was limited by space charge in the amorphous (multi) layers for this part of the characteristics. In the fourth part of the characteristics at high biases, the current was limited by the series resistance.

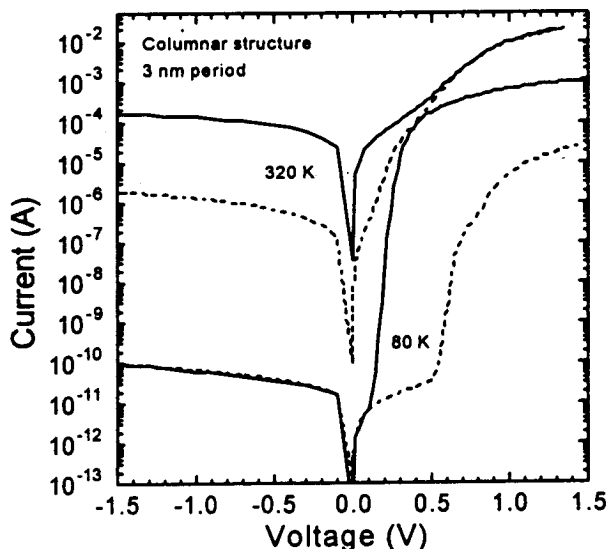


Fig. 1. Forward and reverse I-V characteristics of two different diodes (solid and dashed lines, respectively) prepared on the same wafer with SiGe multilayers of columnar structure (0 V bias) obtained at 80 and 320 K.

It was also found that there are at least three parallel paths for the current flow through the amorphous layers sputtered from Si and Ge targets. One is the parallel hopping conductance at low current

levels mentioned above as the first part of the forward I-V characteristics. The second path is through the Schottky barrier. However, there is a third path as well exhibiting large ohmic leakage currents at room temperatures in a part of the diodes, and rectifying properties with low Schottky barrier height at low temperatures, as can be seen in Fig. 1. (The reverse characteristics of both type of diodes is determined with the parallel hopping conductance at low temperatures, as presented in Fig. 1 for 80 K.) This path is probably connected with defects (weak points) in the amorphous layers.

The temperature dependence of the most abrupt (second) part of the I-V characteristics attributed to a Schottky barrier, were different for the different type of structures [17]. Amorphous SiGe layers exhibited increasing ideality factors with decreasing temperature. This feature is characteristic for usual Schottky junctions as well and is attributed either to the lateral inhomogeneity of the Schottky barrier height or to that thermionic-field emission dominates the current through the junction [15]. Amorphous multilayers exhibited a constant ideality factor of around 3 at low temperatures. This can be connected with the localization of charge carriers in the Ge layers at temperatures below 220 K, resulting in a sharp decrease of the diffusion length [18]. Polycrystalline SiGe layers showed a constant ideality factor of around 2 at temperatures below 220 K [17]. The latter has to be connected with the domination of generation current at low temperatures.

The C-V characteristics of amorphous structures exhibited a maximum for forward biases [1,14,16]. This behaviour is connected either with the charge transfer from and to the potential wells formed by the sputtered layers, or with the effect of the high series resistance at high current levels.

A very good correlation has been obtained between the electrical behaviour and the optical absorption. The absorption of the amorphous Si/Ge multilayers and amorphous and polycrystalline SiGe layers at a photon energy of around 1 eV correlated very well with the apparent free hole concentration evaluated from the room temperature C-V measurements for the studied wafers [17]. The origin of

this correlation is that both the optical absorption at these energies and the capacitance of the structures are directly related to band tail states.

The amorphous SiGe layers sputtered from a SiGe target exhibited similar I-V characteristics with four different parts as obtained for the multilayered and mixed layers sputtered from Si and Ge targets. With increasing thickness of the amorphous SiGe layer the I-V characteristics of the p-type structures ("Acetone" treatment) became worse: the current due to hopping conductivity increased and the part of I-V characteristics limited by space charge became more dominant. The "HF" treatment increased the apparent Schottky barrier height for p-type and decreased for n-type structures [14].

The hydrogenated amorphous structures exhibited I-V characteristics depending on the temperature very weakly. At low current levels there was an exponential I-V relationship, which saturated at higher current levels. The I-V characteristics in this region exhibited a quadratic dependence of the current on the bias [6] indicating space-charge limited current. A new type of heterodiodes was proposed on the basis of these results [6].

B. Epitaxial SiGe layers and Multilayered SiGe/Si Structures

On the monocrystalline SiGe structures the effect of surface treatment was studied by using a HF and a $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ procedure. In an earlier work, the HF treatment yielded a Schottky barrier height of 0.76 eV for n-type Si, while the $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ treatment resulted in a barrier height less than 0.15 eV (i.e. very good ohmic behaviour) [9]. For n-type SiGe, the HF treatment yielded a Schottky barrier height of 0.73 eV, which is close to the value obtained for n-Si. But the barrier height obtained for the " $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ " treatment has been 0.46 eV, which is much higher, than that for n-Si. This indicates that in contrary to Si, this treatment does not passivate the SiGe surface [2]. On the other hand, this higher value of barrier height can also be connected with that the current through the structure is limited by a potential barrier at the SiGe/Si interface. An extended misfit

dislocation network has been detected at the SiGe/Si interface by cross-sectional transmission electron microscopy [19]. Positively charged deep levels originated from defects yield a triangular potential barrier at this interface.

Due to the defects at the SiGe/Si interface, the electrical behaviour exhibited different anomalies. Forward I-V characteristics showed excess currents. For junctions with "HF" treatment a strong increase of reverse current was obtained for the reverse bias range of 0.1-0.3 V. This strong bias dependence indicates a recharging process within the junction which affects the barrier height [2]. C-V characteristics exhibited very strong temperature dependence for the studied junctions with " $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ " treatment. There was also a fast change of the capacitance near zero bias, which also indicates a recharging process close to the Al/SiGe interface. These junctions exhibited high conductance at room temperature as well. Further on, the C-V characteristics exhibited a switching behaviour with a hysteresis at moderate forward biases [2]. Nevertheless, the free electron profiles evaluated from the C-V characteristics of both types of junctions ("HF" and " $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ " treatments) were very similar [2,19]. This indicates that the profiles obtained for junctions with low barrier height are also reliable, so one can obtain information about the region closer to the semiconductor surface. Indeed, a peak was obtained in the apparent free electron profile at 0.2 μm which corresponds to the misfit dislocation network at the SiGe/Si interface. So, the junctions with two different Schottky barrier heights proved to be a very useful tool for studying the structures [2,19].

In the case of n-SiGe/p-Si and HEMT structures [16], the surface treatment affected the vertical electrical behaviour very strongly, as presented in Fig. 2 for an n-SiGe/p-Si structure.

In the experiment with $\text{ErSi}_{1.7}$ epitaxial layers, the structure with Si capping layer exhibited ohmic behaviour at room temperature with a contact resistivity of about 1 Ωcm , but at low temperatures it showed rectifying behaviour. The structure without capping layer exhibited rectifying behaviour even at room temperature. The temperature dependence of the forward current was weak for both contacts. The

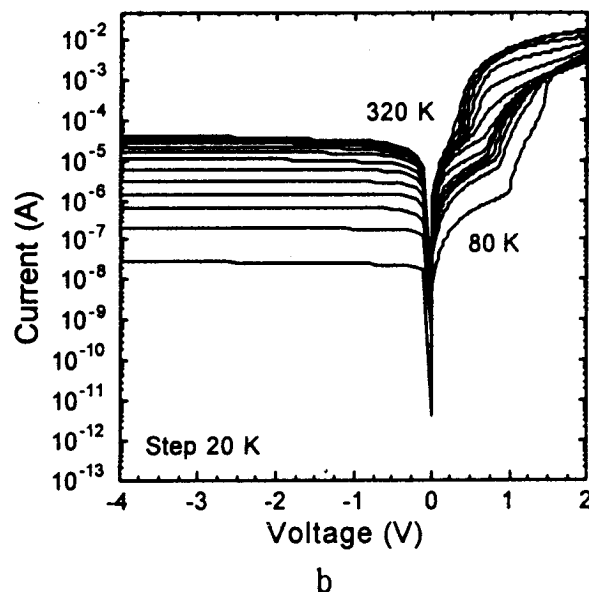
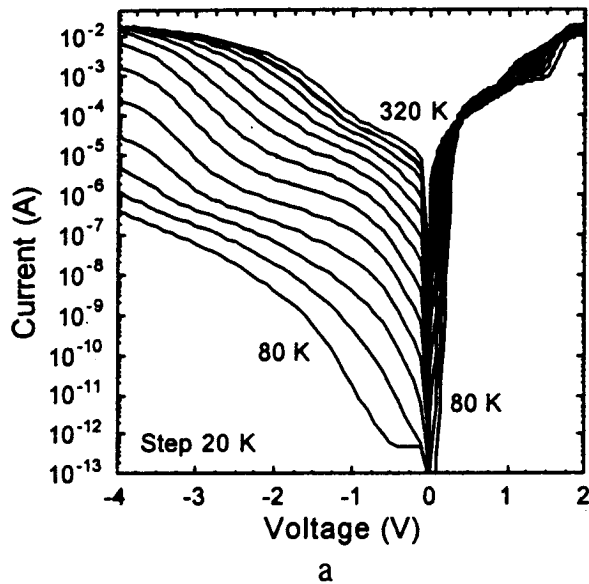


Fig. 2. Forward and reverse I-V characteristics of Al/n-SiGe/p-Si structures prepared with "HF" (a) and " $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ " (b) treatment from the same wafer, as a function of temperature.

forward current was ohmic at low current levels in both structures, but it was due to space-charge limited mechanism at low temperatures and high current levels.

Memory effect also has been obtained at low temperatures [13].

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