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Electrical peculiarities in Al/Si/Ge/. . ./Ge/Si and Al/SiGe/Si structures

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Abstract

The current–voltage (*I–V*) and capacitance–voltage (*C–V*) behaviour of different Si/Ge multilayers and SiGe single layers prepared on p-type Si substrates by magnetron sputtering and annealing, has been studied in the temperature range of 80–320 K by using Al Schottky contacts as test structures. Although a significant influence of the microstructure of the Si/Ge multilayers and SiGe layers was obtained on the electrical behaviour of the structures, the structures exhibited similar specific features.

Keywords: Si; SiGe; Schottky barrier; Superlattice; Amorphous; Electrical behaviour

1. Introduction

Amorphous Si/Ge multilayers were grown on p-type Si substrate by dc magnetron sputtering. The deposition of the films was assisted with ion irradiation (controlled by negative substrate bias). The films grown without bias exhibited columnar structure. With application of ion irradiation, an optimum bias was determined to suppress the columnar growth structure, and amorphous SiGe alloy formation was observed at more energetic ion bombardment. Intermixed SiGe amorphous and polycrystalline films were also achieved by annealing of the sputtered multilayers.

The microstructure and morphology of the as-deposited and annealed layers were investigated by cross-sectional transmission electron microscopy and X-ray diffraction measurements in earlier works [1,2]. In this work Al Schottky contacts have been prepared to the structures and their vertical electrical characteristics were studied by current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements. Although a significant influence of the microstructure of the sputtered and annealed layers was obtained on the electrical behaviour of the structures, the structures exhibited similar specific features, as outlined below.

2. Experimental

The amorphous Si/Ge multilayers were grown in a dual target unbalanced magnetron dc sputtering system [1,2]. The 2 in. diameter planar magnetrons were tilted 25° with respect to the substrate surface normal and had a focus point 10 cm from the target surfaces where the substrate table was positioned.

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Table 1
The substrate potential, annealing conditions, layer structure, apparent barrier heights obtained from the *C–V* and *I–V* measurements, and the ideality factor for the studied structures

Wafer	Bias (V)	Annealing	Structure	ϕ_{bC} (eV)	ϕ_{bI} (eV)	n
L1	0	–	a-Si/a-Ge	0.63 ± 0.03	0.71 ± 0.01	1.24 ± 0.01
L2	140	–	a-Si/a-Ge	0.67 ± 0.02	0.68 ± 0.01	1.73 ± 0.15
M1	450	–	a-SiGe	0.67 ± 0.02	0.68 ± 0.01	1.17 ± 0.06
M2	140	650 °C, 10 min	Poly-SiGe	0.73 ± 0.06	0.57 ± 0.02	1.82 ± 0.15
M3	450	600 °C, 10 min	a-SiGe	0.77 ± 0.03	0.62 ± 0.02	1.96 ± 0.41

All multilayers were grown on p-type Si(0 0 1) wafers with the native oxide remaining. The Si substrates were ultrasonically cleaned (in trichloroethylene, acetone and ethanol) and blown dry with nitrogen gas immediately before introducing them into the chamber through a load-lock system. Prior to growth the vacuum chamber was evacuated to a pressure below 6.7×10^{-5} Pa (5×10^{-7} Torr). As sputtering gas 99.9997% pure Ar was used. The targets were operated in constant current mode, typically at 140 mA (Si) and 40 mA (Ge), which gave target potentials of approximately −500 V. This resulted in growth rates of ~0.1 nm/s as measured with a dual-head quartz crystal. During growth the substrates were kept at ambient temperature and on a negative substrate potential (bias). In front of each magnetron a computer controlled shutter was positioned. All depositions started with a 5 min pre-sputtering of the targets with both shutters closed. Starting with Si, the shutters were then opened and closed to form the desired multilayer. Between each layer both shutters were closed for 0.25 s.

The multilayers were grown to a total thickness of 0.3 μm with a period of 3 nm (100 periods), and were always terminated with an a-Si layer. Three different bias values were used during sputtering: 0, 140 and 450 V. According to our earlier measurements performed by cross-sectional transmission electron microscopy, sputtering at zero bias yielded amorphous multilayers with pronounced columnar microstructure, i.e. low density films with well-defined layers at the column boundaries. Sputtering at a bias of 140 V resulted in more dense and well-defined amorphous multilayers, while almost homogeneous intermixed amorphous SiGe layers were obtained by sputtering at a bias of 450 V [1,2].

A structure grown at a bias of 140 V was annealed at 650 °C for 10 min in forming gas. Due to this annealing step, a polycrystalline SiGe layer was obtained with an average grain size of approximately 50 nm [2]. Another structure grown at a bias of 140 V, was annealed at 600 °C also for 10 min in forming gas. Due to our earlier measurements, this structure remained amorphous. The experimental details are summarised in Table 1.

Al was evaporated on both the front and backside of the wafers for the formation of Schottky and Ohmic contacts, respectively. Square diodes with an area of 0.64 mm^2 were formed on the front side of the wafers by standard photolithography.

I–V and 1 MHz *C–V* measurements were carried out at room temperature (10 diodes per wafer) and in the temperature range of 80–320 K (two to four diodes per wafer) in dark. The *I–V* characteristics were evaluated for thermionic emission by using an effective Richardson constant value of 32 A/cm^2 K^2 used for p-type Si.

3. Results and discussion

A significant influence of the microstructure of the Si/Ge multilayers and SiGe layers was obtained on the electrical behaviour of the structures, as it can be seen in Fig. 1 that presents the typical forward *I–V* characteristics measured at room temperature on all of the studied structures. However, the structures exhibited similar specific features. As a common picture, forward *I–V* characteristics consisted of four different parts as shown in Fig. 2a for wafer L1 (amorphous multilayers with columnar structure), while the *I–V* characteristics of a usual Schottky junction consist of two parts only, as presented in Fig. 2b for an Al/p-Si junction for comparison. On this wafer a chemical treatment of the Si surface was performed before the

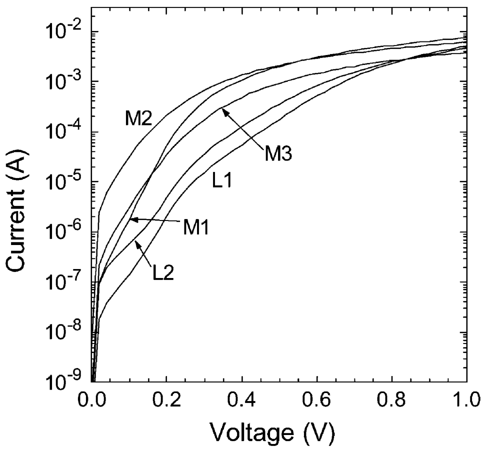

Fig. 1. Typical room temperature forward *I–V* characteristics of the studied structures.

evaporation of the Al Schottky layer using a 1:20 HF:H_2O solution for 10 s [3]. (These junctions exhibited a Schottky barrier height of 0.52 ± 0.01 eV and an ideality factor of 1.11 ± 0.03 in the temperature range of 140–320 K.)

Concerning the *I–V* characteristics of the studied structures (Figs. 1 and 2a), the central, most abrupt part is attributed to a Schottky barrier formed by Al on the sputtered layers. The first part at low biases showed Ohmic behaviour and is connected with a parallel conductance through probably some defects in the sputtered layers. The third part exhibiting a linear log *I–V* relationship with a lower slope at relatively high biases, was obtained for multilayers only (see Fig. 1). So, in this part, the current is limited by the conductance of the sputtered multilayers. In the fourth part at high biases, the current is limited by the series resistance. The different parts of the forward *I–V* characteristics appeared at different temperatures for the different structures. For example, the mixed amorphous and polycrystalline layers did not contain the parallel Ohmic component at room temperature (see Fig. 1), it appeared for these structures at low temperatures only. Further on, some *I–V* characteristics indicated lateral inhomogeneity, i.e. the presence of two or more phases with different Schottky barrier height and different series resistance. This effect can be seen in Fig. 2a for temperatures 100–180 K. The forward *I–V* curves for these temperatures are double-step-like.

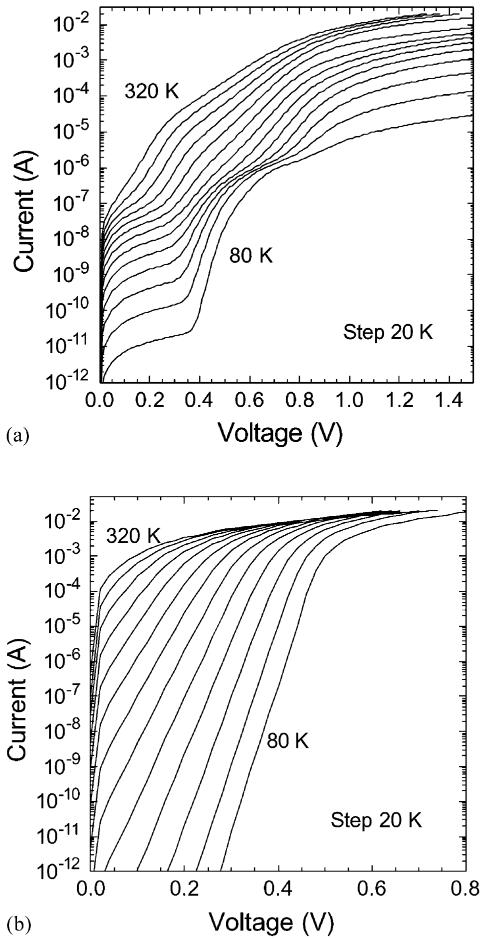

Fig. 2. Typical forward *I–V* characteristics obtained in the temperature range of 80–320 K by steps of 20 K for wafer L1 (amorphous multilayers with columnar structure) (a), and for an Al/p-Si Schottky junction with HF surface treatment (b).

The effect of microstructure was monitored by evaluating the ideality factor and the apparent Schottky barrier height [4] from the *I–V* and *C–V* characteristics. The obtained values are presented in Table 1.

The best performance was obtained for wafer M1 with intermixed amorphous SiGe layer. It exhibited an apparent Schottky barrier height of 0.67 ± 0.02 eV obtained from both measurements with an ideality factor of 1.17 ± 0.06. The same apparent barrier heights were obtained for wafer L2 with perfect amorphous Si/Ge superlattice. However, the ideality factor in this case was much higher (1.73 ± 0.15). Wafer L1 with columnar amorphous superlattice structure exhibited higher apparent barrier height evaluated from the *I–V*, and lower one, evaluated from the *C–V* measurements. However, annealed structures (M2 and M3) behaved just opposite. They exhibited much lower apparent barrier height evaluated from the *I–V*, and much higher one, evaluated from the *C–V* measurements. These changes have to be connected with the change of the conduction band discontinuity and of the charge stored in the sputtered layers.

The high ideality factor for wafer L2 can be connected in part with the potential drop on the Si/Ge superlattice or SiGe layer, and mainly with the fact that the current range limited by the Schottky contact is about one and a half order of magnitude only for this structure at room temperature (see Figs. 1 and 2a). The lower this current range the higher the ideality factor [5,6]. In general, this effect is due to the superposition of an additional (parallel) current mechanism at low biases (e.g. generation current, leakage, etc.), and an additional potential drop on another junction, resistance, etc. at high biases, which is connected in series with the Schottky junction [5,6]. The excess current at low biases and the potential drop at high biases affect the slope of the abrupt part significantly, if it is not long enough. This is, why the ideality factor for wafer L2 is much higher, than for L1 and M1. The current range limited by the Schottky contact is much lower for wafer L2 due to higher leakage currents and to the potential drop on the superlattice.

The high ideality factors of annealed wafers has to be connected to other mechanism which is not clear yet. Perhaps lateral inhomogeneity or additional interface states were created during annealing [4].

The apparent barrier heights evaluated from the *C–V* measurements are very close to those obtained from the *I–V* measurements for samples L2 and M1. The difference for the other samples must be connected with the charge stored in the superlattice and with the doping level of the SiGe layer different from that of the substrate [4,7].

C–V characteristics also exhibited specific behaviour as presented in Fig. 3 for wafer L2. Relatively large excess capacitance was obtained for positive forward biases at low temperatures in all the studied structures, which is not observed for usual Schottky junctions with good performance. This excess capacitance can be connected with the charge transfer from and to the potential wells formed by the sputtered layers, or with deep levels (interface states) in the amorphous and polycrystalline layers [8–10].

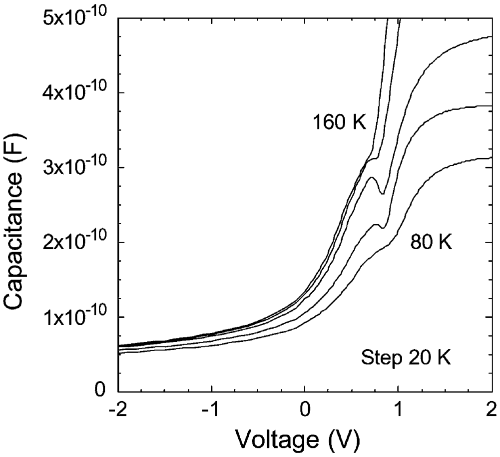

Fig. 3. Unusual *C–V* characteristics obtained in the temperature range of 80–160 K by steps of 20 K for wafer L2 (amorphous multilayers with perfect structure).

4. Conclusions

The *I–V* and *C–V* behaviour of different Si/Ge multilayers and SiGe single layers prepared on p-type Si substrates by magnetron sputtering and annealing, has been studied in the temperature range of 80–320 K by Al Schottky contacts as test structures. A significant influence of the microstructure of the Si/Ge multilayers and SiGe layers was obtained on the electrical behaviour of the structures. However, the structures exhibited similar specific features. Forward *I–V* characteristics consisted of four different parts corresponding to different current mechanisms. *C–V* characteristics exhibited excess capacitance for forward biases that can be connected with the charge transfer from and to the potential wells formed by the sputtered layers, or with deep levels in them.

Acknowledgements

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