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Vertical Electrical Behaviour of GaAs and Si Based Low Dimensional Structures

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A brief summary of unusual vertical electrical behaviour obtained in different epitaxial GaAs/InAs/GaAs, amorphous, polycrystalline and epitaxial Si/Ge/Si and Si/SiGe/Si, and porous Si/crystalline Si low dimensional structures is given.

INTRODUCTION

The development of semiconducor technology led to structures and devices containing very small objects, namely thin layers, thin wires and small dots with characteristic dimensions in the range of a few nm. The part of these structures, where there is a quantum confinement of charge carriers in the small objects, is called low (two-, one- or zero-) dimensional structures, while the small objects themselves are called quantum wells, quantum wires and quantum dots, respectively [1-3]. On the other hand, the quantum confiment of charge carriers can perform also in structures that do not contain small objects. E.g., in metal-oxide-semiconductor and different heterostructures it can be due to bending of the conduction or valence band edges at interfaces [1-4]. Moreover, quantum confiment can be obtained even in the same semiconductor material using delta doped layers [1-3,5,6]. All the structures exhibiting quantum confiment of charge carriers, are considered low dimensional.

The optical behaviour of low dimensional structures are widely studied due to their importance for optoelectronic diveces [1-3,7]. Concerning their electrical properties, mainly their lateral electrical and magnetotransport behaviour are studied [1-3,8]. This is connected with their importance for high electron mobility transistors (HEMTs), on one hand, and with quantum mechanical effects obtained in these structures, on the other hand.

The vertical electrical behaviour of low dimensional structures has been studied much less [9,10]. Most of these works was devoted to double barrier resonant tunneling structures for their practical importance. However, the vertical electrical behaviour of low dimensional structures are also worth to study. They exhibit specific features characteristic for the actual structure. In this paper our experimental results exhibiting unusual vertical electrical behaviour of different GaAs/InAs/GaAs, Si/Ge/Si, Si/SiGe/Si, and porous Si/Si low dimensional structures, are briefly summarized.

EXPERIMENTAL

GaAs/InAs/GaAs Structures

InAs/GaAs quantum well (QW) and self-aggregated quantum dot (QD) structures were grown on n-GaAs substrates by Molecular Beem Epitaxy (MBE) and Atomic Layer MBE (ALMBE) [11-13]. Au Schottky contacts were formed on the top and AuGeNi ohmic contact on the back side of the wafers. Three different structures were studied as

Au Schottky contact
ALMBE n-GaAs cap layer (0.4 µm, 2×10^{16} cm^{-3})
MBE n-GaAs buffer layer (1 µm, 2×10^{16} cm^{-3})
n^+-GaAs substrate
AuGeNi ohmic contact

a

Au Schottky contact
MBE n-GaAs cap layer (0.6 µm, 2×10^{16} cm^{-3})
ALMBE n-GaAs confining layer (0.4 µm, 2×10^{16} cm^{-3})
InAs QW (1 monolayer)
MBE n-GaAs buffer layer (1 µm, 2×10^{16} cm^{-3})
n^+-GaAs substrate
AuGeNi ohmic contact

b

Au Schottky contact
MBE n-GaAs cap layer (0.6 µm, 2×10^{16} cm^{-3})
ALMBE n-GaAs confining layer (0.4 µm, 2×10^{16} cm^{-3})
InAs QDs (3 monolayers)
MBE n-GaAs buffer layer (1 µm, 2×10^{16} cm^{-3})
n^+-GaAs substrate
AuGeNi ohmic contact

c

Fig. 1: The studied InAs/GaAs reference Schottky (*a*), QW (*b*), and QD (*c*) structures

shown in Fig. 1: a reference Schottky (no InAs layer), a QW (1 monolayer InAs) and a QD (3 monolayer InAs) structure [14]. Details of preparation see in Refs. [11-14].

Al ohmic or Schottky contact, relatively to n-Si (#4121 or #4122, respectively)
10 nm n-Si
40 nm n-$Si_{0.82}Ge_{0.18}$ (1×10^{17} cm^{-3})
10 nm undoped $Si_{0.82}Ge_{0.18}$
10 nm undoped Si
200 nm undoped $Si_{0.82}Ge_{0.18}$
300 nm p-$Si_{0.82}Ge_{0.18}$ (1×10^{16} cm^{-3})
100 nm p-Si
n-Si substrate (1×10^{16} cm^{-3})
Al ohmic contact

Fig. 2: The studied Si/SiGe/Si HEMT structure with ohmic (#4121) and Schottky (#4122) top contacts

Si/Ge/Si and Si/SiGe/Si Structures

Amorphous, polycrystalline and epitaxial Si/Ge/Si and Si/SiGe/Si structures were prepared. Concerning amorphous structures, a-Si/a-Ge multi-layers were grown on p-type moncrystalline Si wafers in a dual target unbalanced magnetron dc. sputtering system. As sputtering gas, pure Ar was used. The multilayers were grown to a total thicknesses of 0.3 µm with a period of 3 nm (100 periods), and were always terminated with an a-Si layer. Three different bias values were used during sputtering: 0, 140 and 450 V. According to our earlier measurements performed by cross-sectional transmission electron microscopy [15,16], sputtering at zero bias yielded amorphous multilayers with pronounced columnar microstructure, i.e. low density films with well-defined layers at the column boundaries. Sputtering at a bias of 140 V resulted in more dense and well-defined amorphous multilayers, while almost homogeneous intermixed amorphous SiGe layers were obtained by sputtering at a bias of 450 V [1]. A structure grown at a bias of 140 V was annealed at 650 ^{o}C for 10 min in forming gas. Due to this annealing step, a polycrystalline SiGe layer was obtained with an average grain size of approximately 50 nm. Another structure grown at a bias of 140 V,

was annealed at 600 ^{o}C also for 10 min in forming gas. Due to our earlier measurements, this structure remained amorphous [15-16]. For more details of preparation see Refs. [15-18].

The epitaxial structures were grown by MBE with solid phase Si and gas phase GeH_4 sources. Simple SiGe/Si sructures with a Ge content in the range of 0.11-0.20 and HEMT structures (see Fig. 2) were grown. For more details see Refs. [17,19,20].

Al Schottky contacts and Al ohmic contacts were formed on the top and back sides of the wafers by using the same Al evaporation, but different preceeding chemical treatment of the Si surface for obtaining ohmic or Schottky contact [21,22]. For HEMT structures both ohmic and Schottky contacts were prepared on the top side of the wafers.

Porous Si/Si Structures

Porous silicon (PS) layers were formed by anodization of (100) oriented n, p and p^+ Si wafers in different electrolytes containing HF, ethanol and water [23-26]. On the top of the PS layers gold contacts were formed by sputtering, while the back-side ohmic contacts were prepared by ion-implantation and evaporation of Al. No passivation of the porous layer was performed.

Measurements

Most of the wafers were studied by current-voltage (I-V) and 1 MHz capacitance-voltage (C-V) conductance-voltage (G-V) measurements carried out at room temperature (10 diodes per wafer) and in the temperature range of 80-320 K or 80-360 K with steps of 20 K (2-4 diodes per wafer) in dark. PS structures were studied by C-V and G-V measurements at room temperature only.

RESULTS AND DISCUSSION

GaAs/InAs/GaAs Structures

Although QW and QD layers were relatively far from the Au/GaAs interface out of the equilibrium depletion depth of the Schottky junction, it was observed that QDs affected the electrical behaviour of the structures much more, than QWs [12,13]. Concerning the I-V characteristics, the structures with QDs showed lower apparent Schottky barrier height and much larger series resistance, than the reference structure and the structures with QW (12-14,27).

Further on, an excess current was observed in all the studied QD structures at low temperatures and low current levels, while no excess current was present for QW structures. The excess current in the QD structures was different for each individual diodes and unstable exhibiting instabilities with changing the bias, as it is presented in Fig. 3, and over the time [14,27]. We explained the excess current by an additional minority injection current which is connected with recombinationof charge carriers through the defect levels connected with the formation of QDs [14,27].

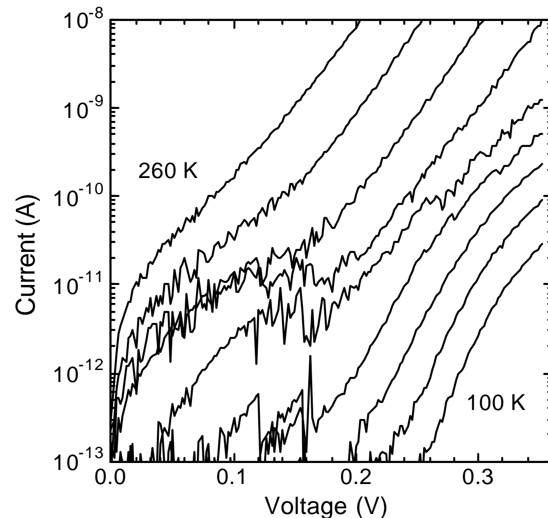


Fig. 3: Excess currents in a GaAs/InAs/GaAs QD structure measured in the temperature range of 100-260 K with temperature steps of 20 K and voltage steps of 2 mV.

Concerning C-V behaviour, QW and QD structures exhibited step like C-V characteristics [12,13], and peeks in the corresponding G-V curves, as presented in Fig. 4 for a QD structure. The effect

is more pronounced at low temperatures. The evaluated apparent doping profiles contained wide peaks and deeps [12]. These features are connected with charge escape from QW and QDs with increasing the reverse bias [10]. For QD structures the capacitance and conductance depended strongly on the frequency. QDs affected the breakdown behaviour of the junctions as well: they exhibited much stronger temperature dependence of the breakdown voltage, than that of the reference and QW structures [13,28].

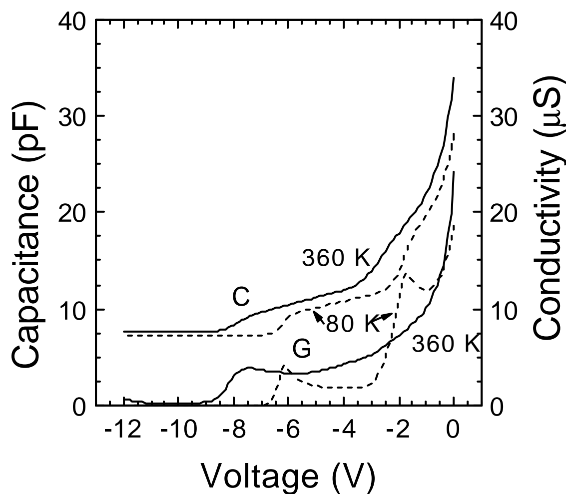


Fig. 4: C-V and G-V characteristics of a GaAs/InAs/GaAs QD structure measured at the temperatures of 80 and 360 K.

Si/Ge/Si and Si/SiGe/Si Structures

Although a significant influence of the microstructure of Si/Ge multilayers and SiGe layers was obtained on the electrical behaviour of the structures, the structures with amorphous and polycrystalline layers exhibited similar specific features. As a common picture, forward I-V characteristics consisted of four different parts as shown in Fig. 5. for the wafer with amorphous multilayers of columnar structure. The central, most abrupt part is attributed to a Schottky barrier formed by Al on the sputtered layers. The first part at low biases showed ohmic behaviour: it is connected with a parallel conductance through probably some defects in the sputtered layers. In the third part exhibiting a linear logI-V relationship with a lower slope at relatively high biases, the current is limited by the conductance of the sputtered layers. In the fourth part at high biases, the current is limited by the series resistance. The different parts of the forward I-V characteristics appeared at different temperatures for the different structures. Some I-V characteristics indicated lateral inhomogeneity, i.e. the presence of two or more phases with different Schottky barrier height and different series resistance. This effect can be seen in Fig. 5. for temperatures 100-180 K. The forward I-V curves for these temperatures are double-step-like.

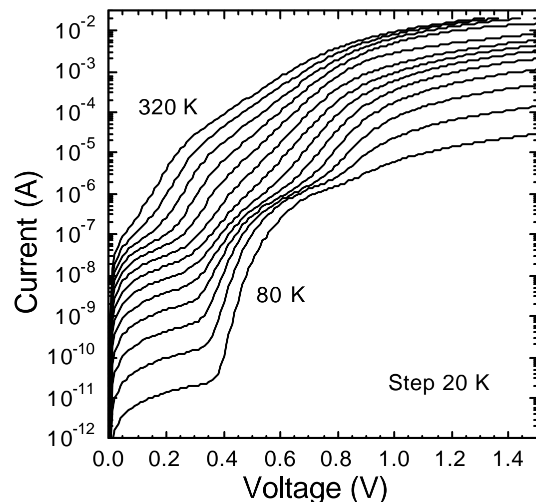
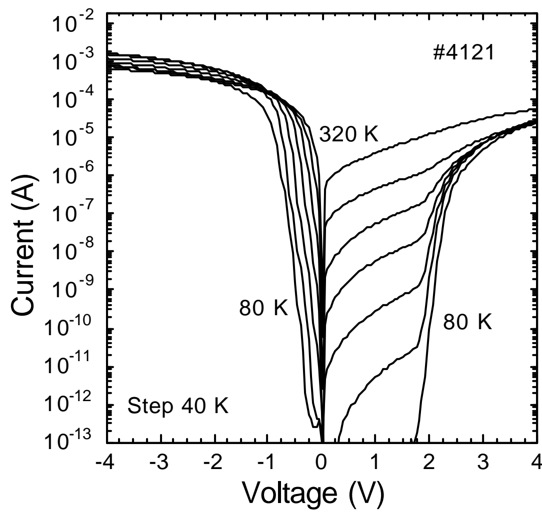


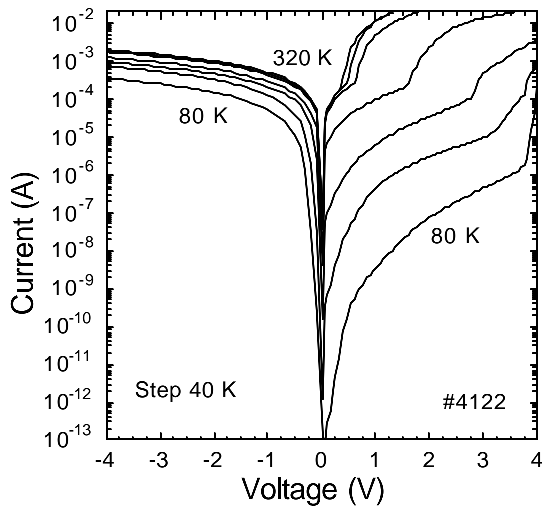
Fig. 5: Typical forward current-voltage characteristics obtained in the temperature range of 80-320 K by steps of 20 K for the wafer with amorphous multilayers of columnar structure

While the epitaxial SiGe/Si structures exhibited usual Schottky-like I-V behaviour [17], the vertical I-V characteristics of HEMT structures were also strange, as shown in Fig. 6. Structures with ohmic and Schottky top contacts exhibited much different

I-V behaviour. The origin of this large difference is not understood yet.



a



b

Fig. 6: Typical vertical current-voltage characteristics obtained in the temperature range of 80-320 K by steps of 40 K for HEMT structures with ohmic (*a*) and Schottky (*b*) top contacts (the voltage sign is relative to the top contact)

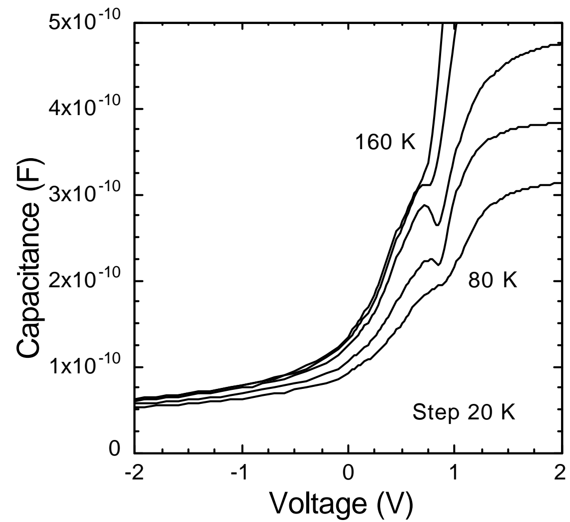


Fig. 7: Unusual capacitance-voltage characteristics obtained in the temperature range of 80-160 K by steps of 20 K for wafer with amorphous multilayers of perfect structure

The C-V characteristics of the structures with sputtered layers also exhibited specific behaviour as presented in Fig. 7 for wafer amorphous multilayers of perfect structure. Relatively large excess capacitance was obtained for positive forward biases at low temperatures in the studied amorphous and polycrystalline structures, which is not observed for usual Schottky junctions with good performance. This excess capacitance is probably connected with deep levels in the amorphous and polycrystalline layers [29-31]. The excess capacitance can also be due to charge escape from potential wells formed by layers with different band gaps. Similar behaviour was obtained in the HEMT structures, but no excess capacitance was observed in the epitaxial SiGe/Si structures.

Porous Si/Si Structures

In all of the studied PS structures the C-V behaviour was similar to that of poor metal-insulator-semiconductor capacitors [22,32]. Both the C-V and G-V characteristics exhibited a hysterezis, as it is

shown in Fig. 8 for an n-type PS structure. These results indicate that a part of the porous layer

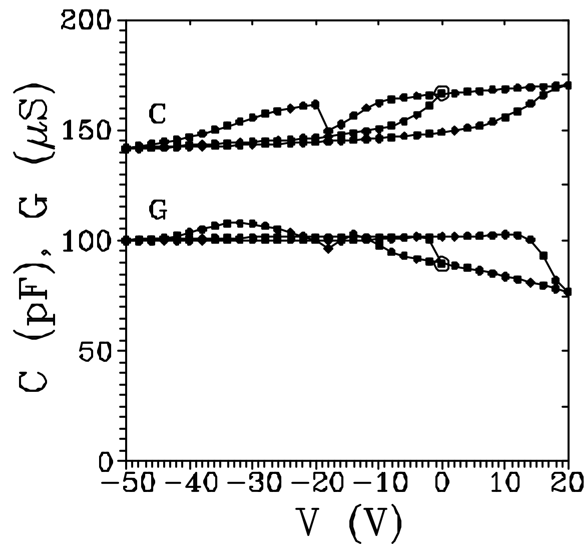


Fig. 8: C-V and G-V characteristics typical for Au/PS/n-Si structures containing a sponge-like PS layer with an average porosity of 0.55 and thickness of 1.8 μm. The device area is 4.0 mm^2. The bias was changed by steps of 2 V, the capacitance was measured in 1 s after applying the bias. Circles indicate the starting point. The structure was biased first to negative voltages, than to positive and negative voltages again. The fast changes of capacitance and conductance were obtained after changing the direction of biasing.

behaves like an insulator at the measurement frequency, but there is a slow charge exchange in this part of the PS layer resulting in the hysterezis.

The obtained normalized "insulator" capacitance values decreased with increasing porosity for both the sponge-like and columnar structures [22]. Above a porosity of 60% the whole PS layer behaved as an insulator. (Details see in Ref. [22].)

The direction of the hysterezis loops was opposite for n- and p-type structures [32]. Their actual directions indicated that the charge exchange yielding the hysterezis, took place between the PS layer and Si substrate for n-type structures, while between the PS layer and Au for p-type structures [32]. This implies that the hysterezis loop is due to electron capture and release into and from the PS layer, respectively. Consequently, the PS layer contains electron traps. In general, the obtained C-V characteristics changed in long-term scale [22,32]. In some cases we obtained that the hysteresis became gradually narrower with aging, and disappeared finally.

The most interesting observation was a reproducible characteristic switching phenomenon in structures prepared on the n-type wafer with a porosity of 0.55 [32]. As it is seen in Fig. 8., during the C-V measurements, when decreasing the reverse bias from -20 to -18 V, the capacitance dropped rapidly to near its minimal value, indicating a rapid charge exchange between the porous silicon layer and the silicon substrate at -18 V. Simultaneously, there was also a similar change in the conductivity at this bias, as it is also seen in Fig. 8. Unfortunately, these features decreased drastically with aging, and disappeared in five weeks along with the hysteresis behaviour. The change in the conductivity remained observable longer than that in the capacitance.

The observed switching phenomenon was perhaps connected with resonant tunneling of electrons into and through the crystallites in the porous layer. The room temperature air-oxidation of the sidewalls of crystallites with aging might change the allowed energy levels in them (decreasing their dimensions), on one hand, and block the charge exchange between them (decreasing the tunneling probability by isolation), on the other hand, yielding the disappearance of the switching phenomenon and of the hysteresis.

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